ABSTRACT OF THE DISCLOSURE

The semiconductor regions for source and drain of unused p-channel type MISFETQp and the power supply wiring 2VDD are electrically connected and the semiconductor regions for source and drain of n-channel type MISFETQn and the power supply wiring 2VSS are electrically connected. Moreover, the switch elements 3SW1, 3SW2 are formed of the p-channel type MISFETQp and n-channel type MISFETQn in the basic cells and these switch elements 3SW1, 3SW2 are discretely arranged in the n-well NWL and p-well PWL. Thereby, noise generated in the wells can be reduced in the semiconductor device where the switch elements are provided between the power supply wiring and wells and the threshold voltage of transistor formed in the well can be controlled through the ON/OFF controls of such switch elements.